

Analog Output Specifications

Table 1 lists the analog output specifications for the DT9850 Series modules.

Table 1: Analog Output Specifications

Description	Feature	Specifications
General DAC Specifications	Number of analog output channels DT9853 and DT9853-M: DT9854 and DT9854-M:	4 8
	Resolution	16 bits
	Data encoding (input)	Offset binary
	Nonlinearity (integral)	± 4 LSB typical
	Differential linearity	± 1 LSB (monotonic)
	Throughput (full scale) Single value:	1 kHz update rate for a single channel, typical (system dependent)
	Isolation to the host computer	± 300 V

Table 1: Analog Output Specifications (cont.)

Description	Feature	Specifications
Voltage Output Specifications	Output range (@3.5 mA, 2.8 k Ω)	± 10 V, 0 to 10 V (software configurable)
	Output transient ± 10 V to (0 to 10 V) or (0 to 10 V) to ± 10 V range selection: Host is reset, powered on, suspended, or a reset command is issued to the device: Initial power on:	Duration: 5 μ s typical; Amplitude: 5 V p-p typical Duration: 50 ms typical; Amplitude: 0.5 V peak typical Duration: 50 ms typical; Amplitude: 0.5 V peak typical
	Zero error	Software-adjustable to zero
	Gain error	± 15 LSBs maximum
	Output impedance	0.3 Ω typical
	Output coupling	DC
	Capacitive drive capability	0.001 μ F minimum (no oscillations)
	Protection	Short Circuit to Analog Common
	Power-on voltage	0 V ± 10 mV maximum
	Settling time to 0.01% of FSR	10 μ s, 20 V step
	Slew rate	2 V/ μ s

Table 1: Analog Output Specifications (cont.)

Description	Feature	Specifications
Current Output Specifications	Current output	±3.5 mA maximum (10 V/2.8 kΩ)
	Current output sink	0 to 20 mA
	Compliance voltage range	+8 VDC to +36 VDC ^a
	Absolute accuracy Resistive load = 100 Ω	±0.05% of full-scale range
	Leakage current (all 0s written to current output channels)	100 nA maximum (for each current output channel)

- a. Use the following equation to determine the maximum voltage to use at the load:

$$U_{load_max} = (\text{Compliance voltage} - 8 \text{ V}) / 0.02 \text{ A}$$

Digital I/O Specifications

Table 2 lists the digital input and digital output specifications for the DT9850 Series modules.

Table 2: Digital Input and Digital Output Specifications

Feature	Specifications
Digital logic type	CMOS
Number of lines	8 digital inputs (port B); 8 digital outputs (port A)
Digital I/O transfer rate	Up to 1 kHz (system dependent)
Power on and reset state	Digital input
Pull-up/pull-down configuration:	User-configurable on inputs ^a ; By default, all input pins floating
Digital input loading	TTL (default) 47 k Ω (pull-up/pull-down configuration)
Inputs Input type: Input load: High-level input voltage: Low-level input voltage: Interrupt-on-change:	Level sensitive Schmitt trigger 3.5 V minimum 1.5 V maximum Digital input lines 0 to 6
Outputs Output driver: Output driver high voltage: Output driver low voltage:	Push-pull logic 4.3 V minimum (IOH = -2 mA); 0.6 V maximum (IOL = 10 mA)

- a. For pull-up, connect the Digital I/O Termination Select pin to the +5 V Out pin. For pull-down, connect the Digital I/O Termination select pin to the Digital Ground pin.

Counter/Timer Specifications

Table 3 lists the specifications for the C/T subsystem.

Table 3: C/T Subsystem Specification

Feature	Specifications
Number of counter/timer channels	1
Resolution	32
Counter mode	Event counting
Input type	TTL, rising-edge trigger
Maximum input frequency	1 MHz
Minimum pulse width	
High:	500 ns
Low:	500 ns
Schmidt trigger hysteresis	20 mV to 100 mV
Input leakage current	$\pm 1.0 \mu\text{A}$ typical
Input high voltage	4.0 V minimum, 5.5 V absolute maximum
Input low voltage	1.0 V maximum, -0.5 V absolute minimum

DAC_Sync Trigger Specifications

Table 4 lists the specifications for the DAC_Sync trigger signal.

Table 4: DAC_Sync Trigger Specification

Feature	Specifications
Power on and reset state	Input
Termination	Internal 100 k Ω pull-down
Software-selectable direction Input ^a :	Receives DAC_Sync signal from external source
Output ^b :	Outputs internal DAC_Sync signal
Clock pulse width Input:	1 μ s minimum
Output:	5 μ s minimum
Input leakage current	± 1.0 μ A typical
Input high voltage	4.0 V minimum, 5.5 V absolute maximum
Input low voltage	1.0 V minimum, -0.5 V absolute minimum
Output high voltage ^c IOH = -2.5 mA:	3.3 V minimum
No load:	3.8 V minimum
Output low voltage IOH = 2.5 mA:	1.1 V maximum
No load:	0.6 V maximum

- a. When you configure the trigger source for the module as external, the DAC_Sync signal is configured as an input (the default configuration). When a low-to-high transition is detected on the DAC_Sync pin, the module simultaneously updates its analog output channels.
- b. When you configure the trigger source for the module as software, the DAC_Sync signal is configured as an output. When you start an operation (using a software command), the module outputs a signal on the DAC_Sync pin.
- c. DAC_Sync is a Schmitt trigger input is over-current protected with a 200 Ω series resistor.

Power, Physical, and Environmental Specifications

Table 5 lists the power, physical, and environmental specifications for the DT9850 Series modules.

Table 5: Power, Physical, and Environmental Specifications

Feature	Specifications
Power +5 V: +5 V Output:	±0.5 V@ 500 mA maximum 10 mA (isolated)
Physical Dimensions: Weight:	100 mm x 100 mm 65.79 g
Environmental Operating temperature range DT9853 and DT9854: DT9853-M and DT9854-M: Storage temperature range: Relative humidity: Altitude:	0° C to 70° C 0° C to 50° C -40° C to 85° C to 90%, noncondensing up to 10,000 feet

Regulatory Specifications

Table 6 lists the regulatory specifications for the DT9850 Series modules.

Table 6: Regulatory Specifications

Feature	Specifications
Emissions (EMI)	FCC Part 15, EN55022:1994 + A1:1995 + A2:1997 VCCI, AS/NZS 3548 Class A
Immunity	EN61000-6-1:2001
RoHS (EU Directive 2002/95/EG)	Compliant (as of July 1st, 2006)